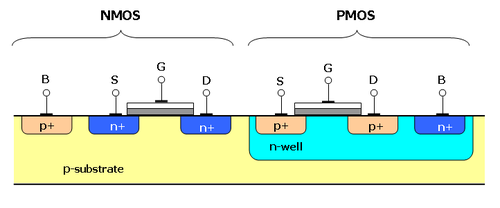
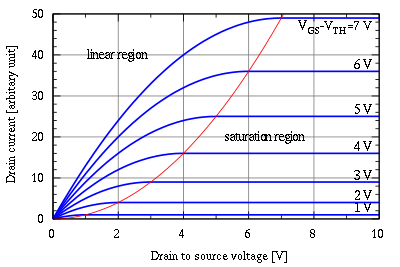
**Simplified NMOS and PMOS Structure**



**Drain-Source Current Versus Drain-Source voltage**



**Drain-Source Current in Triode region**

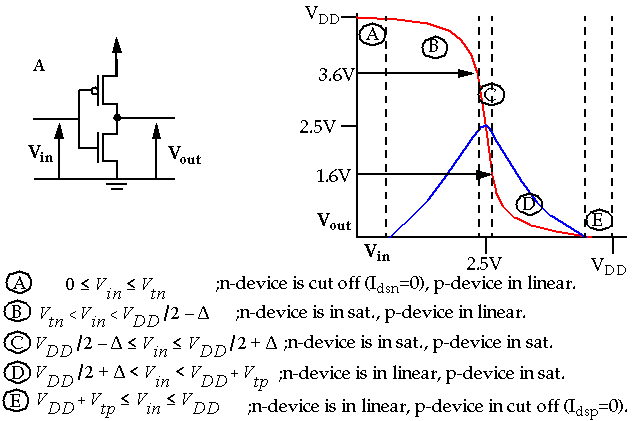
I_D= \mu_n C_{ox}\frac{W}{L} \left( (V_{GS}-V_{th})V_{DS}-\frac{V_{DS}^2}{2} \right)

**Drain-Source Current in Saturation region**

I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{th})^2 \left(1+\lambda (V_{DS}-V_{DSsat})\right).

**Transfer characteristics of an inverter**

At each region we should look at the relation between Vds and (Vgs -Vth)

****

**Why is the substrate in NMOS connected to Ground and in PMOS to VDD?**   
We try to reverse bias not the channel and the substrate but we try to maintain the drain, source junctions reverse biased with respect to the substrate so that we don’t lose our current into the substrate.   
  
**What is the fundamental difference between a MOSFET and BJT?**  
BJT is a current controlled device and MOSFET is a voltage controlled device.   
BJT is a current controlled device as the input current is amplified subjected to the mode of operation. For example in CE mode the input current is base current and output current is emitter current which is (β+1) times amplified.

MOSFET is a voltage controlled device like JFET where there is metal oxide in between the gate and the channel. Depending on the voltage supplied on the gate terminal a voltage is 'induced' by electrostatic induction in the isolated channel.

**Which transistor has higher gain, BJT or MOS and why?**   
BJT has higher gain because it has higher trans-conductance. This is because the current in BJT is exponentially dependent on input where as in MOSFET it is square law.   
  
**In CMOS technology, in digital design, why do we design the size of PMOS to be higher than the NMOS?**   
In PMOS the carriers are holes whose mobility is less than the electrons, the carriers in NMOS. That means PMOS is slower than an NMOS. In CMOS technology, NMOS helps in pulling down the output to ground and PMOS helps in pulling up the output to Vdd. If the sizes of PMOS and NMOS are the same, then PMOS takes long time to charge up the output node. If we use a larger PMOS then there will be more carriers to charge the node and overcome the slow nature of PMOS. Basically we do all this to get equal rise and fall times for the output node.   
  
**Why PMOS and NMOS are sized equally in a Transmission Gates?**   
In Transmission Gate, PMOS and NMOS aid each other rather competing with each other. That's the reason why we need not size them like in CMOS. In CMOS design we have NMOS and PMOS competing which is the reason we try to size them proportional to their mobility.   
  
**All of us know how an inverter works. What happens when the PMOS and NMOS are interchanged with one another in an inverter?**   
If the source and drain are also connected properly. It will act as a buffer. But suppose input is logic 1 output will be degraded 1 similarly degraded 0;